PERSONAL INFORMATION

Name: **Shady Agwa**

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QUALIFICATIONS

2018 **PhD in Electronics Engineering,** The American University in Cairo, Egypt.

2011 **MSc in Computer Engineering,** Assiut University, Egypt.

2006 **BSc in Computer & Systems Engineering,** Assiut University, Egypt.

CURRENT POSITION

2022 - Present **Research Fellow** *in* **ASIC-driven AI Architectures**
Centre for Electronic Frontiers, School of Engineering, The University of Edinburgh, UK.

PAST POSITIONS

2021 - 2022 **Senior Research Fellow** *in* **AI Hardware Design**
Centre for Electronic Frontiers, University of Southampton, UK.

2019 - 2021 **Postdoctoral Associate** *in* **Computer Architecture & Digital VLSI**
Computer Systems Lab, Cornell University, USA.

2018 **Postdoctoral Researcher** *in* **Digital VLSI**
Center of Nanoelectronics & Devices, The American University in Cairo AUC, Egypt.

2012 - 2018 **Research & Teaching Assistant**
Center of Nanoelectronics & Devices, Zewail City of Science & Technology ZC, Egypt.

GRANTS

Jan. 2024 **"ProSensing: Low-Power, High-Speed, Adaptable Processing-In-Sensing Capability"**
UKRI EPSRC National Security Sandpit 2, Budget: £1,457,851.00, 3 Years.
Themis Prodromakis (PI) and ***Shady Agwa (Research Co-I)***, University of Edinburgh. Eiman Kanjo (Co-I), Nottingham Trent University. Antonio Hurtado (Co-I), University of Strathclyde.

PATENTS

2023 **"A Memory Computing Device, a Method of Operating the Same and an AI System Including the Same"** Inventors: ***Shady Agwa*** and Themis Prodromakis. **PCT App. No. PCT/GB2024/05052.**

2023 **"An Associative Memory Element and Peripheral Circuitry Arrangement"** Inventors: Alex Serb, Yihan Pan, ***Shady Agwa***, Mohammed Mughal, Adrian Wheeldon, Sachin Maheshwar, and Themis Prodromakis. **PCT App. No. PCT/GB2023/05324.**

In Progress

2024 **"Unconventional Weight Stationary Systolic Array for Matrix-Matrix Multiplication"** Inventors: **Shady Agwa**, Ahmed J. Abdelmaksoud and Themis Prodromakis. Edinburgh Innovation Disclosure Form EI0000871.

2024 **"Triangular Input Movement Systolic Array for Convolutional Neural Networks"** Inventors: Cristian Sestito, **Shady Agwa** and Themis Prodromakis. Edinburgh Innovation Disclosure Form EI0000872.

2024 **"TXL-ACAM Cell"** Inventors: Georgios Papandroulidakis, **Shady Agwa** and Themis Prodromakis. Edinburgh Innovation Disclosure Form EI0000858.

CHIPS (TAPE-OUTs)

2023 **Analog Content-Addressable Memory ACAM, FORTE RUN-3,** RRAM and TSMC 180nm**:** University of Edinburgh, UK.

2022	**Characterisation Platform for RRAMs, FORTE RUN-2,** TSMC 180nm**:** University of Southampton/ Edinburgh & Imperial College London, UK.
2020	**Coherent Interconnect & FPGA Enabling Reuse, CIFER,** GF 12nm**:** Cornell University & Princeton University, USA.
2015	**Power Efficient AES Encryption Core,** UMC 130nm**:** The American University in Cairo, Egypt.
2014	**Resilient Power Efficient 16-bit MAC Unit,** GF 65nm**:** The American University in Cairo, Egypt.

TEACHING ACTIVITIES

2023 - 2024	**Digital Systems Lab Courses (4th & MSc)**, The University of Edinburgh, UK.
2014 - 2018	**Advanced Topics in Electronics Engineering** (Teaching Assistant), The American University in Cairo, Egypt.
2017	**EDA for Physical Design and Algorithms** (Teaching Assistant), Zewail City of Science & Technology, Egypt.
2015 - 2017	**Digital ASIC Design Flow**, The American University in Cairo, Egypt.

TALKS & WORKSHOPS

Oct. 2023	**"Bridging The Gap Between Emerging Technologies And AI Hardware,"** ***Invited Speaker*** at 8th European Congress on Advanced Nanotechnology and Nanomaterials, London, UK.
Aug. 2023	***Organizer*** of **"ASIC-BASIC"**, 3-day Workshop for MSc. Students at **University of Edinburgh** on Basics of Digital ASIC Design using open-source Skywater 130nm PDK.

CO-ADVISING/MENTORING

Postdoctoral Associates	**1- Dr. Georgios Papandroulidakis,** RRAM-based Analogue Template Matching for Energy Efficient Edge Classification. **2- Dr. Cristian Sestito,** Convolution Neural Networks CNNs Acceleration using Systolic Arrays for ASIC & FPGA-SoC. **3- Dr. Yihan Pan,** Digital In-memory Computing Architectures for Matrix Multiplication Acceleration.
PhD Students	**1- Ahmed Abdelmaksoud,** AI Hardware Acceleration for Natural Language Processing (NLP) Models using Systolic Arrays for Digital ASIC.
MSc. Students	**1- Yikang Shen, 2023,** Digital In-Memory Computing using Stochastic Data Representation. **2- Junyang Shu, 2023,** Systolic Arrays Exploration for Convolution Layer Acceleration. **3- Weijie Huang, 2023**, RRAM-based Convolutional Neural Networks (CNNs) Simulator using NeuroPack. **4- Xiangyi Yin, 2023**, RRAM-based Acceleration for Convolutional Neural Networks (CNNs).

RECENT PROJECTS

2023 - Present	**AI Hardware Architectures for NLP Models (Transformers):** *The University of Edinburgh, UK.*
2021 - Present	**Digital In-memory Stochastic Computing Architectures:** *The University of Edinburgh, UK.*
2023 - Present	**CNN Hardware Accelerators:** *The University of Edinburgh, UK.*
2022 - Present	**Analog Content-Addressable Memory CAM for Edge Classification:** *The University of Edinburgh, UK.*
2021 - 2022	**Memristors Characterization Platform:** *The University of Edinburgh & Imperial College London, UK.*
2021 – 2022	**Symbolic-Level Computing using Associative Memories:** *The University of Edinburgh, UK.*
2020 – 2021	**Digital In-memory Computing Architecture using Emerging SOTFET Device:** *Cornell University, USA.*

2020 - 2021 **Multi-Core Implementation for CIFER Chip:** *Cornell University & Princeton University, USA.*

2019 – 2021 **Digital In-SRAM Computing :** *Cornell University, USA.*

2019 – 2020 **Hammer-Blade Manycore Evaluation:** *Cornell University & University of Washington, USA.*

PUBLICATIONS

Journals (refereed):

- Cristian Sestito, **Shady Agwa** and Themis Prodromakis," TrIM: Triangular Input Movement Systolic Array for Convolutional Neural Networks—Part II: Architecture and Hardware Implementation", Submitted to **IEEE Transactions on Circuits and Systems I, TCASI**, 2024.

- Cristian Sestito, **Shady Agwa** and Themis Prodromakis,"TrIM: Triangular Input Movement Systolic Array for Convolutional Neural Networks—Part I: Dataflow and Analytical Modelling", Submitted to **IEEE Transactions on Circuits and Systems I, TCASI**, 2024.

- Pan, Yihan, Adrian Wheeldon, Mohammed Mughal, **Shady Agwa**, Themis Prodromakis and Alexantrou Serb, "An Energy-efficient Capacitive-Memristive Content Addressable Memory." arXiv **2024**: arXiv-2401. (submitted to **TCASI**).

- Ang Li, Ting-Jung Chang, Fei Gao, Tuan Ta, Georgios Tziantzioulis, Yanghui Ou, Jinzheng Tu, Kaifeng Xu, Paul Jackson, August Ning, Grigory Chirkov, Marcelo Orenes-Vera, **Shady Agwa**, Xiaoyu Yan, Eric Tang, Jonathan Balkind, Christopher Batten, David Wentzlaff, "CIFER: A Cache-Coherent 12nm 16mm2 SoC With Four 64-Bit RISC-V Application Cores, 18 32-Bit RISC-V Compute Cores, and a 1541 LUT6/mm2 Synthesizable eFPGA," in **IEEE Solid-State Circuits Letters**, August **2023**, doi: 10.1109/LSSC.2023.3303111.

- **S. Agwa** and T. Prodromakis, "Digital in-memory stochastic computing architecture for vector-matrix multiplication" **Frontiers in Nanotechnology**, Nanoelectronics Section, 5:1147396, **2023**. doi: 10.3389/fnano.2023.1147396.

- **S. Agwa**, E. Yahya and Y. Ismail, "A Low Power Self-healing Resilient Microarchitecture for PVT Variability Mitigation ", in **IEEE Transactions on Circuits and Systems I**: Regular Papers, vol. 65, no. 6, pp. 1909-1918, June 2018, doi: 10.1109/TCSI.2017.2771821.

- **S. Agwa**, E. Yahya and Y. Ismail, "ERSUT: A Self-Healing Architecture for Mitigating PVT Variations without Pipeline Flushing", in **IEEE Transactions on Circuits and Systems II**: Express Briefs, vol. 63, no. 11, pp. 1069-1073, Nov. 2016, doi: 10.1109/TCSII.2016.2548261.

- **S. Agwa**, E. Yahya and Y. Ismail, "Design techniques for variability mitigation", International Journal of Circuits and Architecture Design, Vol. 1, No. 1. Pp. 20-40, 2013. https://doi.org/10.1504/IJCAD.2013.057450.

Conferences (refereed): ** = Prestigious Conferences for Computer Architectures & Systems*

- Cristian Sestito, Weijie Huang, **Shady Agwa** and Themis Prodromakis, "PyT-NeuroPack: A Hybrid PyTorch/Memristor-Crossbar Simulation Tool for Convolutional Neural Networks,", 2024 IEEE Interregional NEWCAS Conference, NEWCAS, 2024.

- **Shady Agwa** and Themis Prodromakis, "Bridging The Gap Between Emerging Technologies And AI Hardware," 8th European Congress on Advanced Nanotechnology and Nanomaterial's, London UK, October **2023**.

- **Shady Agwa** and Themis Prodromakis, "Bent-Pyramid: Towards A Quasi-Stochastic Data Representation for AI Hardware," 2023 21st IEEE Interregional NEWCAS Conference (NEWCAS), Edinburgh, United Kingdom, **2023**, pp. 1-5, doi: 10.1109/NEWCAS57931.2023.10198194.

- *** Shady Agwa**, Georgios Papandroulidakis and Themis Prodromakis, "A 1T1R+2T Analog Content-Addressable Memory Pixel for Online Template Matching," 2023 IEEE International Symposium on Circuits and Systems (**ISCAS**), Monterey, CA, USA, **2023**, pp. 1-5, doi: 10.1109/ISCAS46773.2023.10181451.

- ***** Ting-Jung Chang, Ang Li, Fei Gao, Tuan Ta, Georgios Tziantzioulis, Yanghui Ou, Moyang Wang, Jinzheng Tu, Kaifeng Xu, Paul Jackson, August Ning, Grigory Chirkov, Marcelo Orenes-Vera, **Shady Agwa**, Xiaoyu Yan, Eric Tang, Jonathan Balkind, Christopher Batten, and David Wentzlaff, "CIFER: A 12nm, 16mm2, 22-Core SoC with a 1541 LUT6/mm2, 1.92 MOPS/LUT, Fully Synthesizable, Cache- Coherent, Embedded FPGA," 2023 IEEE Custom Integrated Circuits Conference (**CICC**), San Antonio, TX, USA, **2023**, pp. 1-2, doi: 10.1109/CICC57935.2023.10121294.

- ***** Khalid Al-Hawaj, Tuan Ta, Nick Cebry, **Shady Agwa**, Olalekan Afuye, Eric Hall, Courtney Golden, Alyssa B. Apsel and Christopher Batten, "EVE: Ephemeral Vector Engines", 2023 IEEE International Symposium on High-Performance Computer Architecture (**HPCA**), Montreal, QC, Canada, **2023**, pp. 691-704, doi: 10.1109/HPCA56546.2023.10071074..

- ***** Andrea Mifsud, Jiawei Shen, Peilong Feng, Lijie Xie, Chaohan Wang, Yihan Pan, Sachin Maheshwari, **Shady Agwa**, Spyros Stathopoulos, Shiwei Wang, Alexander Serb, Christos Papavassiliou, Themis Prodromakis and Timothy G. Constandinou, "A CMOS-based Characterisation Platform for Emerging RRAM Technologies," 2022 IEEE International

Symposium on Circuits and Systems (**ISCAS**), Austin, TX, USA, **2022**, pp. 75-79, doi: 10.1109/ISCAS48785.2022.9937343.

- *** S. Agwa**, Y. Pan, T. Abbey, A. Serb and T. Prodromakis, "High-Density Digital RRAM-based Memory with Bit-line Compute Capability," 2022 IEEE International Symposium on Circuits and Systems (**ISCAS**), Austin, TX, USA, **2022**, pp. 1199-1200, doi: 10.1109/ISCAS48785.2022.9937848.

- O. Afuye, **S. Agwa**, C. Batten and A. Apsel, "Layout-Based Evaluation of Read/Write Performance of SOT-MRAM and SOTFET-RAM," ESSDERC 2021 - IEEE 51st European Solid-State Device Research Conference (ESSDERC), 2021, pp. 283-286, doi: 10.1109/ESSDERC53440.2021.9631814.

- ***** K. Al-Hawaj, O. Afuye, **S. Agwa**, A. Apsel and C. Batten, "Towards a Reconfigurable Bit-Serial/Bit-Parallel Vector Accelerator using In-Situ Processing-In-SRAM," 2020 IEEE International Symposium on Circuits and Systems (**ISCAS**), Seville, Spain, 2020, pp. 1-5, doi: 10.1109/ISCAS45731.2020.9181068.

- Y. Ou, **S. Agwa** and C. Batten, "Implementing Low-Diameter On-Chip Networks for Manycore Processors Using a Tiled Physical Design Methodology," 2020 14th IEEE/ACM International Symposium on Networks-on-Chip (NOCS), 2020, pp. 1-8, doi: 10.1109/NOCS50636.2020.9241710.

- C. Tan, Y. Ou, S. Jiang, P. Pan, C. Torng, **S. Agwa** and C. Batten, "PyOCN, a unified framework for modeling, testing, and evaluating on- chip networks," 2019 IEEE 37th International Conference on Computer Design (ICCD), Abu Dhabi, United Arab Emirates, 2019, pp. 437-445, doi: 10.1109/ICCD46524.2019.00068..

- *** S. Agwa**, E. Yahya and Y. Ismail, "Power efficient AES core for IoT constrained devices implemented in 130nm CMOS," 2017 IEEE International Symposium on Circuits and Systems (**ISCAS**), Baltimore, MD, USA, 2017, pp. 1-4, doi: 10.1109/ISCAS.2017.8050361.

- **S. Agwa**, E. Yahya and Y. Ismail, "Variability Mitigation Using Correction Function Technique," 2013 IEEE 20th International Conference on Electronics, Circuits, and Systems (ICECS), Abu Dhabi, United Arab Emirates, 2013, pp. 293-296, doi: 10.1109/ICECS.2013.6815412.

- **Shady O. Agwa**, Hany h. Ahmad and Awad I. Saleh, "Hardware Pessimistic Run-Time Profiling for A Self-Reconfigurable Embedded Processor Architecture," 2010 International Conference on Reconfigurable Computing and FPGAs, Cancun, Mexico, 2010, pp. 162-167, doi: 10.1109/ReConFig.2010.12.

- **Shady O. Agwa**, Hany h. Ahmad and Awad I. Saleh, "Towards A Self-Reconfigurable Embedded Processor Architecture," 2009 International Conference on Computer Engineering & Systems, Cairo, Egypt, 2009, pp. 21-26, doi: 10.1109/ICCES.2009.5383316.

Theses:

- **S. Agwa**, "Power efficient resilient microarchitectures for PVT variability mitigation", PhD thesis, The American University in Cairo AUC, 2018.

- **Shady O. Agwa**, " Towards A Self-Reconfigurable Embedded Processor Architecture", MSc. thesis, Assiut University, 2011.